Attorney Docket No. T2147-908627

RESPONSE UNDER 37 C.F.R. 1.116
EXPEDITED PROCEDURE – EXAMINING GROUP 2128

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ANE 1/ entered W/RCE dtd 8/20/07

In re Patent Application of:

First Named Inventor: KASZYNSKI, Anne

Art Unit: 2128

Appln. No.: 10/627,976

Examiner: Alhija, Saif A.

Filed: July 28, 2003

Confirmation No.: 4095

For: Method for Functional Verification of an Integrated Circuit Model in Order to Create A Verification Platform, Equipment Emulator and Verification Platform

Do Not Enter SA 8/23/07

McLean, Virginia
August 20, 2007

AMENDMENT AFTER FINAL REJECTION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of April 20, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 12 of this paper.